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| 09/945,495 | 08/30/2001 | Fernando Gonzalez | 303.776US1 | 3528 |

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| EXAMINER | |
|---|---|
| OWENS, DOUGLAS W | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/945,495 | GONZALEZ, FERNANDO | |
| | Examiner | Art Unit | |
| | Douglas W Owens | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sh t with th corr spond nc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *33-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,34,36-41,43,44,46-55,61 and 62* is/are rejected.

7)☒ Claim(s) *35,42,45 and 56-60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claims 40, 41, and 55 – 60 are objected to because of the following informalities:

Claim 40 recites the limitation, "...wherein the source ***or*** drain are bounded by a first STI structure..." (emphasis added). The word "or" in line 5 should be replaced with "and". Claim 41 has the same problem in line 4 of the claim.

Claim 56 requires that "...the recess is covered with a substantially curvilinear bottom profile including epitaxial semiconductive material..." The phrase should be changed to read something like; "...the recess is covered with an epitaxial semiconductive material, wherein said semiconductive material includes a substantially curvilinear profile..." It doesn't make sense to cover a recess with a curvilinear profile. "A curvilinear profile" is descriptive a shape, not a material covering.

Claims 55 and 58 require that the second STI structure is disposed in a direction parallel to the first STI. The scope of the claim cannot be determined since the term "parallel" cannot accurately describe a direction. It is similar to giving a tourist directions by saying that Constitution Avenue is a direction parallel to Independence Ave. The tourist would understand that the two streets do not intersect (definition of parallel lines), but would not know if he/she should travel north or south of Independence Ave. without giving an actual direction of travel.

It seems that the intended scope could be accurately claimed by deleting the phrase, "in a direction".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 39, 40 and 48 – 55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 39, 40, 48 and 49 require that the structure have a minimum photolithographic feature. The scope of the claim is not understood, since it is not known which portion of the structure has the minimum photolithographic feature, nor is it known what limits the size of the feature. Is this limited by the state of the art, requiring the structure to have some feature that is sub micron, or is this the minimum feature that will still provide isolation for the devices?

Claim 50 recites the limitation, "...a first shallow trench isolation (STI) structure disposed in the monocrystalline substrate, wherein the recess exposes at least a portion thereof." The scope of the claim is vague because it is not known if the recess exposes the substrate or the STI. Claims 51 – 55 depend from claim 50, so they are also indefinite.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 33, 34, 36, 37, 38, 41 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 6,239,465 to Nakagawa.

Regarding claim 33, Nakagawa teaches a vertical transistor (Fig. 5, for example), comprising:

a semiconductor substrate comprising an upper surface (Fig. 4D);

a recess disposed in the upper surface (between the STI structures (26)), wherein the recess contains a localized epitaxial semiconductor film (25; Col. 4, line 15) comprising more than three monolithic surfaces (Fig. 4G);

a gate dielectric (33) disposed over the epitaxial film; and

an electrode (34) in the recess over the gate dielectric layer.

Regarding claim 34, Nakagawa teaches a transistor, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

Regarding claim 36, Nakagawa teaches a transistor, wherein the gate dielectric layer is a thermal oxide (Col. 5, lines 38 – 42).

Regarding claim 37, Nakagawa teaches a transistor, wherein the electrode is doped polysilicon (Col. 5, lines 42 – 44).

Regarding claim 38, Nakagawa teaches a transistor, wherein the substrate includes:

an N+ doped source (24; Col. 4, lines 47 – 49) and an N+ doped drain (28; Col. 5, line 25) disposed on opposite sides of the recess (top and bottom).

Regarding claim 41, Nakagawa teaches a vertical transistor, wherein the substrate includes:

an N+ doped source and N+ doped drain on opposite sides of the recess;

wherein the source and drain are bounded by a first STI structure (26);

wherein the source or drain is bounded by a second STI structure;

wherein the recess is disposed in the substrate to first depth (to the source layer); and

wherein the STI structures are disposed in the substrate to a second depth, and wherein the second depth is greater than the first depth.

6. Claims 43, 44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. JP356058267A to Kato et al.

Regarding claim 43, Kato et al. teaches an electrical device comprising (Fig. 2, for example):

a substrate comprising an upper surface;

an active area disposed in the substrate comprising a source (204) and drain (201; See Abstract);

a recess disposed between the source and drain, wherein the recess comprises a substantially curvilinear bottom profile of epitaxial semiconductive material (202; See Abstract);

a gate dielectric layer (206) disposed over the epitaxial semiconductor material; and

an electrode (207) disposed over the gate layer.

Regarding claim 44, Kato et al. teaches an electrical device wherein the electrode has an upper surface that is below the substrate upper surface.

Regarding claim 46, Kato et al. teaches a silicon oxide gate dielectric (see abstract).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 39, 40, 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa.

Regarding claims 39 and 40, as far as indefinite claims can be understood, Nakagawa teaches a vertical transistor, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and

wherein the source and drain are bounded in a first dimension by a first STI structure (26); and

wherein the source or the drain is bounded in a second dimension by a second STI structure.

Nakagawa does not teach an STI structure having a minimum photolithographic feature. The size of isolation structures is subject to optimization, since the size is a result effective variable. It would have been obvious to one of ordinary skill in the art to arrive at the optimal size of the STI through routine experimentation.

Regarding claim 61, Nakagawa teaches a memory system (Figs. 3 and 5 for example; Col. 2, lines 45 – 46) comprising:

an input/output circuit (Fig. 3, Word lines and bit lines);

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains an epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric (33) disposed over the epitaxial semiconductor film; and

an electrode (34) disposed in the recess over the gate dielectric layer.

Nakagawa does not explicitly teach a memory system coupled to a processor. It would have been obvious to one of ordinary skill in the art to couple the memory system taught by Nakagawa to a processor, since the purpose of the memory system is to hold data for processing. This data must be managed by a processor.

Regarding claim 62, Nakagawa does not teach a system, wherein the processor is disposed in a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system and an aircraft. Nakagawa teaches that the memory system can be used for many purposes. The listed purposes are common uses of memory devices and processors. It would have been obvious for one of ordinary skill in the art to use the device in any of these uses since it is desirable to use the device

make marketable and useful products. Additionally, This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963))

9. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al.

Regarding claim 47, Kato et al. teaches an aluminum electrode. Kato et al. does not teach a doped polysilicon electrode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use doped polysilicon for the electrode, since it is a known material that is well suited for the intended use. It is desirable to use electrode materials that can be used to form reliable electrodes. Additionally, the selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

10. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. as applied to claim 43 above, and further in view of US patent No. 6,476,444 to Min.

Kato et al. teaches an electrical device, wherein the substrate includes:

an N+ doped source and N+ doped drain disposed on opposite sides of the recess (top and bottom).

Kato et al. does not teach a source and drain bounded in a first dimension by a first STI structure and bounded by a second STI structure in a second dimension. Min

teaches an electrical device, wherein the substrate includes a source and drain bounded by a first and second STI in a first and second dimension. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Min into the device taught by Kato et al. since it is desirable to prevent unwanted shorting between adjacent active devices.

Neither Kato et al. nor Min teach an STI structure having a minimum photolithographic feature. The size of isolation structures is subject to optimization, since the size is a result effective variable. It would have been obvious to one of ordinary skill in the art to arrive at the optimal size of the STI through routine experimentation.

11. Claims 50 – 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. in view of US patent No. 6,476,444 to Min.

Regarding claim 50, Kato et al. teaches an electrical device comprising (Fig. 2, for example):

a semiconductor substrate including an upper surface;

an active layer disposed in the substrate including a source (204) and drain (201);

a recess between the source and drain;

wherein the recess includes a substantially curvilinear bottom profile comprising epitaxial semiconductor material (see abstract);

a gate dielectric layer (206) disposed over the epitaxial semiconductive material in the recess; and

an electrode (207) I the recess;

and wherein the recess exposes a portion of the substrate.

Kato et al. does not teach a monocrystalline substrate. Monocrystalline substrates are a well known substrate material that is commonly used in the art. It would have been obvious to one of ordinary skill in the art to use a monocrystalline substrate since it is a known material that is well suited for the intended use.

Kato et al. does not teach an STI structure in the substrate. Min teaches an electrical device including an STI structure (27) in the substrate. It would have been obvious to one of ordinary skill in the art to incorporate the STI taught by Min into the electrical device taught by Kato et al. since it is desirable to prevent unwanted shorting between adjacent active devices formed on a substrate.

Regarding claims 51 – 54, Kato et al. does not teach disposing the electrical device in a chip package, wherein the chip package is disposed in a host DRAM module disposed in an electronic system. This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

Regarding claim 55, Kato et al. does not teach an electrical device including a second STI disposed in the substrate in a direction parallel to the first STI. Min teaches an electrical device including a second STI disposed in the substrate in a direction parallel to the first STI. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Min into the device taught by Kato et al. for reasons discussed above.

12. Claims 35, 42 and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

13. Applicant's arguments filed October 2, 2003 have been fully considered but they are not persuasive.

Information Disclosure Statement

The Applicant has requested that the information disclosure statement filed on February 28, 2002 be considered. No such information disclosure statement has been filed.

Drawings

The objection to the drawing is withdrawn.

Claim Objections

The Applicant argues that the language in claims 40 and 41 is correct because the specification and figures disclose that "...a STI structure bounds the source ***and*** the drain...". This is not persuasive since the objection is to the language, "...the source ***or*** drain...". The STI structure does not bound the source or the drain, it bounds both the source and the drain. Therefore, "and" must be used instead of "or".

The Applicant argues that the language of claim 56 is understood to include a recess that has more than three monolithic surfaces. The claim has not been rejected under USC 112, second paragraph for being indefinite, but objected to because of the language. The term, curvilinear can be used to describe a shape or profile, but not a

material that would cover the recess. Claim language such as, "...the recess is covered with epitaxial semiconductive material having a substantially curvilinear profile..." would be more appropriate.

The objection to claims 48 and 49 is withdrawn.

USC 112 Rejections

35 USC 112, second paragraph requires that the specification conclude with one or more claims that point out and distinctly claim the subject matter regarded as the invention. The Applicant argues that the claims are not indefinite because they are described in the DETAILED DESCRIPTION OF THE INVENTION. This is not a convincing rebuttal of a 35 USC 112, second paragraph rejection because the requirement is that the claims point out and distinctly claim the invention. Claims 39, 40, 48 – 50 and 58 are lacking in this regard.

The scope of claims 39, 40, 48 and 49 are nebulous because there is nothing in the claims that lend an understanding what range is included in the "minimum feature". It is agreed that the detailed description of the invention includes discussion of a minimum feature. However, the claims do not particular point out and distinctly claim what dimension or range thereof is included in the minimum feature. With respect to the inquiries that the Applicant considers to be misguided, the purpose of the questions is to demonstrate that is not clear what is meant by "minimum feature".

With respect to claim 50, the Applicant asserts that, "...a plain reading of the claim indicates that the recess exposes at least a portion of the STI...", further stating that "...The recess is in the substrate and inherently exposes the substrate...". It

appears that the Applicant is asserting that the STI **and** the substrate are exposed by the recess. From a plain reading of the claim the term "thereof" in the last line of claim 50 could refer back to one of two subjects, the STI or the substrate. It is once again asserted that the claimed subject matter of claim 50 is not clear. Additionally, the Applicant asserts that the claim requires that the recess be in the substrate, while there is no such limitation. The claim only requires that the recess be disposed between the source and drain.

The Applicant argues that claims 55 and 58 are not indefinite and the Examiner partially agrees since it is clear that the STI structures are disposed in parallel. For this reason the 35 USC 112, second paragraph rejection has been withdrawn and the claims have been objected to because the term "parallel" cannot accurately describe a direction, but does not necessarily rise to the level of a rejection under 35 USC 112. The term parallel is only relevant when considered with another line or surface, not a direction, such as east, west, up, down, to right, etc...

102 rejections

The applicant argues that the epitaxial layer (25) taught by Nakagawa is not localized. See figures 4C to 5, for example show an epitaxial layer that is disposed between isolation trenches 26. It can be seen in the figures that the epitaxial regions are indeed localized to the area between the isolation structures. The applicant further asserts that since the trenches are formed subsequent to the epitaxial layer, it is impossible for the epitaxial layer to be localized. Since the epitaxial region is confined to a local region, it is considered to be localized. The method of fabrication is not

relevant to claims drawn to an apparatus. The patentability of a product does not depend on its method of production.

The Applicant argues that Nakagawa does not teach an electrode having an upper surface below the substrate upper surface. In figure 4B, the device substrate is shown having an upper surface at the top of the epitaxial layer (25). The electrode (34) shown in figures 4G – 5, for example, has an upper surface that is well below the upper surface of the device substrate.

The Applicant argues that Kato does not teach the groove (205) disposed between source (204) and drain (202). In figure 2 it can be seen that the groove lies directly between the source (204) and drain (202). The drain comprises the layer 202, including the portion to the right and below the groove. The groove is directly between this portion of the drain and the source.

The Applicant argues that Kato does not teach an electrode that has an upper surface that is below the substrate upper surface. Where the substrate upper surface is taken to be the upper surface of p-type silicon 203, it can be seen in figure 2 that the electrode has an upper surface below the upper surface of the substrate.

<u>103 rejections</u>

The Applicant argues that the source and drain taught by Nakagawa are not on opposite sides of the recess, but the same side. While the source (24) as a portion on the left side that is also on the same side as the drain (28), there is also a portion of the source that is on the right side of the recess. Moreover, the drain is on the topside of

the trench, and the source is on the bottom side, which can also be referred to as opposite sides.

The Applicant has requested references showing a memory system coupled to a processor, pursuant to MPEP 2144.03. The following references show that memory systems are commonly couple to a processor:

> US patent No. 6,577,010 to Batra et al. teaches a general purpose computer including a memory system coupled to a processor (Col. 5, lines 48 – 58; Fig. 7)
>
> US published patent application No. 2002/0106866 to Chen teaches that a typical processor based system includes a processor coupled to memory (Section [0052]).
>
> US patent No. 6,653,676 to Tsu et al. teaches a processor with a memory device (Col. 8, line 66 – Col. 9, line 6).
>
> US published patent application No. 2002/0130351 to Ghodsi teaches coupling a memory device to a processor (section [0026]; Fig. 1).
>
> Also see US published patent application No. 2002/0154483 to Homer et al. (section [0018]) and US published patent application No. 2002/0168852 to Harshfield et al. (section [0027])

The applicant has requested a reference showing a polysilicon electrode. See Col. 5, lines 42 – 49 of Nakagawa for a discussion of a prior art polysilicon electrode. US patent No. 3,833,919 to Naber (Col. 2, lines 42 – 44) and IBM Technical Disclosure Bulletin, dated march 1, 1972 each disclose conventional polysilicon electrodes.

The Applicant asserts that the previous Office Action was contradictory in stating that the source and drain taught by Kato are on opposite sides of the recess, those opposites sides being the top and bottom. The Examiner fails to see the contradiction.

The source (204) on the upper left side of the recess is on the opposite side of the recess from the portion of the drain (201) on the lower right side of the recess.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). It is desirable in the art to prevent unwanted shorting between adjacent device and it is quite common to provide isolation structures between devices to preserve operational integrity. One having ordinary skill in the art would recognize that it is undesirable for adjacent devices to short together, which would result in unpredicted device operation.

***Conclusion***

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

DWO

EDDIE LEE
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